REMARKS/ARGUMENTS

Brief Summary of Status

Claims 1-55 are pending in the application.

Claims 11-30, 41-45, and 51-55 are allowed.

Claims 1, 5, 9, 31-33, 35, 36, and 46-49 are rejected.

Claims 2-4, 6-8, 10, 34, 37-40 and 50 are objected to.

2. In the above-referenced OA, the Examiner rejected claims 1, 31 and 41 under 35 U.S.C. § 112, 2nd paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which Applicant regards as the invention.

3. In the above-referenced OA, the Examiner objected to claim 41 because of informalities.

4. In the above-referenced OA, the Examiner rejected claims 1, 5, 9, and 31-33 under 35 U.S.C. § 102 (b) as being anticipated by Kohlschmidt (U.S. Patent No. 6,029,061) (hereinafter referred to as "Kohlschmidt").

7. In the above-referenced OA, the Examiner rejected claims 35-36 under 35 U.S.C. § 103 (a) as being unpatentable over Kohlschmidt.

8. In the above-referenced OA, the Examiner rejected claims 46-49 under 35 U.S.C. § 103 (a) as being unpatentable over Kohlschmidt in view of Grundvig (U.S. Patent No. 5,844,435) (hereinafter referred to as "Grundvig").

9. In the above-referenced OA, the Examiner objected to claims 2-4, 6-8, 10, 34, 37-40, and 50 as being dependent upon a rejected base claim, but the Examiner indicated that these claims would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

10. In the above-referenced OA, the Examiner stated that claims 11-20, 21-30, 41-45, and 51-55 are allowed.

Claim Rejections - 35 U.S.C. § 112, 2nd paragraph

2. In the above-referenced OA, the Examiner rejected claims 1, 31 and 41 under 35 U.S.C. § 112, 2nd paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which Applicant regards as the invention.

The Applicant has amended claims 1, 31, and 41 in an effort to clarify more fully the subject matter as claimed by the Applicant.

With respect to the Examiner's comments that "claim 41, line 4-5, the "generating a clock signal using a low power oscillator when he operational mode comprises a low power bypass mode" is not clear why the low power oscillator would be used if it's low power bypass mode." (see OA, Paper No./Mail Date 121204, p. 2).

The Applicant respectfully points out that within the FIG. 7, the FIG. 9, and the FIG. 11, and the associated written specification portions, (among other portions of the Applicant's originally filed written specification and diagrams) depict some possible embodiments that use a low power oscillator when operating in an "LPO Bypass Mode". The Applicant respectfully points out that there are numerous instances within the Applicant's originally filed written specification and diagrams that show how and when a low power oscillator may be employed to generate a clock signal when the operational mode comprises a low power bypass mode.

As such, the Applicant respectfully requests that the Examiner withdraw the rejections to claims 1, 31 and 41 under 35 U.S.C. § 112, 2nd paragraph.

Claim Objections (Informalities)

3. In the above-referenced OA, the Examiner objected to claim 41 because of informalities.

The Applicant has amended claim 41.

As such, the Applicant respectfully requests that the Examiner withdraw the objection to claim 41.

Claim Rejections - 35 U.S.C. § 102 (b)

4. In the above-referenced OA, the Examiner rejected claims 1, 5, 9, and 31-33 under 35 U.S.C. § 102 (b) as being anticipated by Kohlschmidt.

The Applicant respectfully traverses.

With respect to at least one of the limitations of the subject matter as claimed by the Applicant, the Examiner states:

"the clock measurement and processing circuitry is operable to transform the frequency of the received clock substantially to at least one of the frequency of the first clock signal and the frequency of the second clock signal (CSP [103] calibrate the slow clock 102 to the high accuracy clock 101; col. 3, lines 32-40) when the frequency of the received clock signal fails to substantially comprise at least one of the frequency of the

first clock signal and the frequency of the second clock signal." (see OA, Paper No./Mail Date 121204, p. 4).

With respect to FIG. 1 of Kohlschmidt, the Applicant respectfully points out that CSP 103 of the communications terminal 100 must require the delivery of at least 2 clock signals (e.g., the high accuracy clock 101 and the slow clock 102) to support the functionality disclosed therein.

With respect to another of the limitations of the subject matter as claimed by the Applicant, the Examiner states:

"wherein the clock measurement and processing circuitry (105) is operable to receive a clock signal (received clock signals from 101 and 102);" (see OA, Paper No./Mail Date 121204, p. 3).

Throughout Kohlschmidt, it is taught that 2 clock signals are necessary to perform this "calibration" as taught in accordance with Kohlschmidt and s asserted by the Examiner. Several such examples taken from Kohlschmidt are provided to illustrate this point and the need for 2 separate clock signals to determine a "timing relationship" or a "clock relationship" to perform this "calibration functionality."

"Because the high accuracy clock and the slow clock are not synchronized, the CSP and the DSP calibrate the slow clock to the high accuracy clock prior to the terminal entering the sleep mode. During the calibration, a *timing relationship* is calculated by measuring the clock cycles *of each clock source* for a given calibration time interval. Upon terminal wake-up, the *timing relationship* is used to adjust the time-base accordingly." (see Kohlschmidt, col. 2, lines 37-45, *emphasis added*).

"Because the high accuracy clock 101 and the slow clock 102 are not synchronized, the CSP 103 and the DSP 104 calibrate the slow clock 102 to the high accuracy clock 101 prior to the terminal entering the sleep mode. During the calibration, a *timing relationship* is calculated by measuring the clock cycles *of each clock source* for a given calibration time interval. Upon terminal wake-up, the *timing relationship* is used to adjust the time-base accordingly." (see Kohlschmidt, col. 3, lines 32-40, *emphasis added*).

"As such, the DSP 104 reads the contents of the CALACC register to identify a *clock relationship factor between the slow clock 102 and the high accuracy clock 101.*

This factor is used to update the time-base when the terminal 100 enters the wake-up mode from the sleep mode." (see Kohlschmidt, col. 6, lines 51-57, *emphasis added*).

Clearly, any "calibration" as performed by Kohlschmidt requires 2 clock signals. Therefore, the "calibration" of Kohlschmidt cannot possibly be construed as "transforming" of "a received clock signal" to one or more clock signals as claimed by the Applicant.

The subject matter as claimed by the Applicant in claim 1 includes receiving "a clock signal" such that "the clock measurement and processing circuitry is operable to transform the frequency of the received clock signal to at least one of the frequency of the first clock signal and the frequency of the second clock signal when the frequency of the received clock signal fails to comprise at least one of the frequency of the first clock signal and the frequency of the second clock signal."

Kohlschmidt simply does not teach at least this limitation. Kohlschmidt cannot operate when receiving as few as one clock signal. To perform the "calibration" of Kohlschmidt that the Examiner asserts, 2 clock signals are necessarily required. To support this "calibration" functionality as asserted by the Examiner with respect to Kohlschmidt, it is inherently necessary for the use of at least 2 clock signals.

Throughout the Applicant's originally filed written specification and diagrams, it is shown that "one or more" received clock signals may be received by various embodiments of devices including various embodiments of "clock measurement and processing circuitry" included therein (e.g., see FIG. 1 for of the Applicant's disclosure for one such example). Clearly, the Applicant's claimed subject matter includes the situation where 1 received clock signal may be received.

The Examiner cited portions of Kohlschmidt, as well as the general teaching and disclosure of Kohlschmidt simply cannot operate when receiving as few as one clock signal. Kohlschmidt teaches in contradistinction to subject matter as claimed by the Applicant.

Moreover, it is noted that there is no teaching in Kohlschmidt to suggest that the RF 106 (i.e., the Radio Frequency 106) operates using any frequency other than the high accuracy clock 101. Kohlschmidt does not teach any functionality and/or circuitry within the CSP 103 for changing either of the "high accuracy clock 101" or the "slow clock

102" to any other clock for use by the RF 106. There is very little information provided in Kohlschmidt as the "RF 106," so it can easily be provided here for ease of use by the Examiner.

"A radio frequency (RF) segment 106 is coupled to the high accuracy clock 101 and the CSP 103." (see Kohlschmidt, col. 3, lines 14-16).

"Outputs from the CSP 103 and the high accuracy clock 101 are provided to the radio frequency (RF) segment 106." (see Kohlschmidt, col. 4, lines 2-3).

The very diagram of FIG. 1 of Kohlschmidt shows that the "high accuracy clock 101" connects directly to the RF 106. Also, with respect to the connection between the CSP 103 and the RF 106, it appears clear from Kohlschmidt that connection is to shut down/wake up the RF 106 when the terminal enters/exits sleep mode. It is also taught in Kohlschmidt that the RF 106 is actually turned off when the terminal is in sleep mode, and it does not operate using any clock signal at all.

"To initiate low power operations, the communications protocol processor 105 informs the DSP 104 to execute the sleep mode and he DSP 104 similarly informs the CSP 103. The necessary register operations are then implemented by the CSP 103 and the DSP 104 to *disable the high accuracy clock 101 and enter the sleep mode*." (see Kohlschmidt, col. 5, lines 6-11, *emphasis added*).

"During the sleep mode, the time-base of terminal 100 is provided by the slow clock 102 for the duration of the sleep interval which is decremented by the counter in the CSP 103. Therefore, *all components* in the mobile communications terminal 100 may be *shut down* during the sleep mode *except for the slow clock 102 and the portion of the CSP 103 containing the counter*." (see Kohlschmidt, col. 7, lines 36-42, *emphasis added*).

In addition, Kohlschmidt discloses the following with respect to the use of the slow clock during the sleep mode.

"As such, while the terminal is in low power mode, the *slow clock 102 is* <u>*only*</u> *used to maintain the time-base for the terminal*." (see Kohlschmidt, col. 4, lines 55-58, *emphasis added*).

Clearly, it appears that the RF 106 is shut down during the sleep mode (as the RF 106 may certainly be construed as being included within the "all components" that are shut down except for "*except for the slow clock 102 and the portion of the CSP 103*

containing the counter"). Clearly, the "slow clock 102" also is not connected to the RF 106 is sleep mode. It therefore appears that the only clock that is employed by the RF 106, during any operational mode, is the *"high accuracy clock 101," which is connected directly to the RF 106*, and not through the CSP 103.

Also, the Applicant respectfully points out that "calibration," as taught and disclosed within Kohlschmidt, is that functionality of the "slow clock 102" keeping track of what the "high accuracy clock 101" would be if it continued to operate instead of being shut down when the terminal goes into sleep mode. As the "slow clock 102" and the *"portion of the CSP 103 containing the counter"* operate to keep track of what the "high accuracy clock 101" would be for use when a wake up operation occurs within the terminal.

A portion of Kohlschmidt is again provided here to illustrate this point:

"As such, the DSP 104 reads the contents of the CALACC register to identify a *clock relationship factor between the slow clock 102 and the high accuracy clock 101.* This factor is used to update the time-base when the terminal 100 enters the wake-up mode from the sleep mode." (see Kohlschmidt, col. 6, lines 51-57, *emphasis added*).

Kohlschmidt does not teach or disclose that any clock signal that is generated within the CSP 103 that is then provided to and used by the RF 106. Therefore, the Applicant respectfully traverses the Examiner's assertion which appears to be that the CSP 103 is operable to generate any clock that may be used by the RF 106 from either of the "high accuracy clock 101" or the "slow clock 102."

It also appears that the CSP 103 does not determine whether either of the "high accuracy clock 101" or the "slow clock 102" is suitable for use by the RF 106.

This is in contradistinction to the subject matter as claimed by the Applicant.

From at least these comments made above, it is therefore clear that Kohlschmidt fails to teach and disclose each and every element of the subject matter as claimed by the Applicant in claim 1 of a frequency adaptable semiconductor device, comprising: a clock measurement and processing circuitry; a radio frequency circuitry, communicatively coupled to the clock measurement and processing circuitry, that operates using a first clock signal; and a baseband processing circuitry, communicatively coupled to the clock measurement and processing circuitry, that operates using a second clock signal; and

wherein the clock measurement and processing circuitry is operable to receive a clock signal; the clock measurement and processing circuitry determines whether the frequency of the received clock signal comprises at least one of a frequency of the first clock signal and a frequency of the second clock signal; and the clock measurement and processing circuitry is operable to transform the frequency of the received clock signal to at least one of the frequency of the first clock signal and the frequency of the second clock signal when the frequency of the received clock signal fails to comprise at least one of the frequency of the first clock signal and the frequency of the second clock signal."

As such, the Applicant respectfully points out that Kohlschmidt fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant in claim 1.

As such, the Applicant respectfully believes that claim 1 is allowable, and the Applicant respectfully requests that the Examiner withdraw the rejection of independent claim 1 as being anticipated by Kohlschmidt.

With respect to claim 5, the Examiner asserts:

"the measurement circuitry (calibration circuitry, col. 3, lines 32-40) inherently comprises a comparison circuit in order to compare the signal between the slow clock 102 and the high accuracy clock 101 to calibrate the high clock to the slow clock and a microprocessor circuitry (processor within the CSP 103);" (see OA, Paper No./Mail Date 121204, p. 4).

This Examiner cited portion of Kohlschmidt is provided again here.

"Because the high accuracy clock 101 and the slow clock 102 are not synchronized, the CSP 103 and the DSP 104 calibrate the slow clock 102 to the high accuracy clock 101 prior to the terminal entering the sleep mode. During the calibration, a *timing relationship* is calculated by measuring the clock cycles *of each clock source* for a given calibration time interval. Upon terminal wake-up, the *timing relationship* is used to adjust the time-base accordingly." (see Kohlschmidt, col. 3, lines 32-40, *emphasis added*).

The Applicant points out that there is no mention in this Examiner cited portion of Kohlschmidt of any "calibration circuitry." Also, there is no teaching or suggestion of any "comparison" of the "the slow clock 102 and the high accuracy clock 101" in this

Examiner cited portion of Kohlschmidt. In contradistinction, Kohlschmidt teaches and discloses that "the *timing relationship* is used to adjust the time-base accordingly." Also, "*each clock source*" is *measured* to determine the timing relationship between them. The clock sources are not compared by any "comparison circuitry;" in contradistinction, each of them is measured.

As such, the Applicant also respectfully believes that Kohlschmidt fails to teach each and every limitation of the subject matter as claimed by the Applicant in claim 5.

The Applicant also respectfully believes that claims 5, 9, being further limitations on the subject matter as claimed by the Applicant in claim 1, are also allowable.

The Applicant's comments made above are also applicable with respect to claim 31.

The Applicant respectfully asserts that Kohlschmidt fails to teach and disclose each and every element of the subject matter as claimed by the Applicant in claim 31 of a frequency adaptable method, comprising: receiving a clock signal; measuring a frequency of the received clock signal; determining whether the frequency of the received clock signal comprises a frequency that is suitable for use as a baseband processing circuitry main system clock by a baseband processing circuitry; determining whether the frequency of the received clock signal comprises a frequency that is suitable for use as a radio frequency circuitry main system clock by a radio frequency circuitry; processing the received clock signal, when the received clock signal is not suitable for use as the baseband processing circuitry main system clock, to generate a new clock signal that comprises a frequency that is suitable for use as the baseband processing circuitry main system clock; and processing the received clock signal, when the received clock signal is not suitable for use as the radio frequency circuitry main system clock, to generate at least one additional new clock signal that comprises a frequency that is suitable for use as the radio frequency circuitry main system clock.

The Applicant also respectfully believes that claims 32, 33, being further limitations on the subject matter as claimed by the Applicant in claim 31, are also allowable.

As such, the Applicant respectfully requests that the Examiner withdraw the rejections to claims 1, 5, 9, and 31-33 under 35 U.S.C. § 102 (b) as being anticipated by Kohlschmidt.

Claim Rejections - 35 U.S.C. § 103 (a)

7. In the above-referenced OA, the Examiner rejected claims 35-36 under 35 U.S.C. § 103 (a) as being unpatentable over Kohlschmidt.

The Applicant's comments made above are also applicable with respect to claims 35-36.

The Applicant also respectfully believes that claims 35, 36, being further limitations on the subject matter as claimed by the Applicant in claim 31, are also allowable.

As such, the Applicant respectfully requests that the Examiner withdraw the rejections to claims 35-36 under 35 U.S.C. § 103 (a) as being unpatentable over Kohlschmidt.

8. In the above-referenced OA, the Examiner rejected claims 46-49 under 35 U.S.C. § 103 (a) as being unpatentable over Kohlschmidt in view of Grundvig (U.S. Patent No. 5,844,435) (hereinafter referred to as "Grundvig").

The Applicant respectfully traverses.

With respect to at least one of the limitations of the subject matter as claimed by the Applicant in claim 46, the Examiner states:

"determining a frequency of the output signal from the external oscillator (12) when the operational mode of the semiconductor device substantially comprises a low power oscillator mode (when not in power conserve mode, the high accuracy oscillator 12 is measured (col. 2, lines 61-64)." (see OA, Paper No./Mail Date 121204, p. 8).

This Examiner cited portion of Grundvig is provided here:

"Thus, rather than trying to control the absolute frequency of an "on-chip" low power oscillator, the dual clock architecture of the present invention instead allows for frequency variations to be easily measured and accounted for using program control of the processor." (see Grundvig, col. 2, lines 61-64).

The Applicant respectfully points out that this Examiner cited portion of Grundvig also does not describe "determining a frequency of the output signal from the external oscillator (12) when the operational mode of the semiconductor device substantially comprises a low power oscillator mode" as the Examiner seems to assert.

"As will be explained, in a first mode when high accuracy and stability are required, the high accuracy oscillator 12 and external clock 10 may be advantageously chosen as processor clock source. In a second mode when lower power is desired, *the low power oscillator 24 may be chosen as the processor clock source while the <u>high accuracy oscillator 12 is disabled</u>.*" (see Grundvig, col. 3, lines 43-50, *emphasis added*).

Grundvig discloses a first mode (high accuracy and stability) and a second mode (lower power); it appears that the Examiner asserts that the one of these modes that is equivalent to the Applicant's claimed "low power oscillator bypass mode" is Grundvig's first mode (high accuracy and stability).

The Applicant respectfully points out that Grundvig does not teach the limitation of the subject matter as claimed by the Applicant, within claim 46, of "determining whether the frequency of at least one of the generated clock signal and the received clock signal comprises a frequency that is suitable for use as a radio frequency circuitry main system clock by the radio frequency circuitry;"

"Now referring to FIG. 1, there is shown a block schematic of one embodiment of the present invention. As shown, an external clock 10, such as a high accuracy crystal clock source, is *connected via conventional inputs and outputs* to a high accuracy, oscillator 12 on Integrated Circuit (IC) 100. The *interface* to the "off-chip" crystal (external clock) 10 provides the necessary high accuracy *frequency stability* for the high accuracy oscillator 12 *to act as a clock* for the IC 100. A low power oscillator 24 on IC 100 provides an additional "on-chip" low power clock source for the IC 100. According to the present invention, *either* the high accuracy oscillator 12 *in combination with* the "off-chip" crystal (or external clock) 10 *or* the low power oscillator 24 may be selected as the processor clock source to drive a programmable processor 18 under program control. As will be explained, in a first mode when high accuracy and stability are required, the high accuracy oscillator 12 and external clock 10 may be advantageously chosen as processor clock source. In a second mode when lower power is desired, *the low power*

oscillator 24 may be chosen as the processor clock source while the high accuracy oscillator 12 is disabled." (see Grundvig, col. 3, lines 28-50, *emphasis added*).

It is clear that Grundvig intends for the "off-chip" crystal (external clock) 10 and the high accuracy oscillator 12 to act in concert with one another simply to bring the external clock signal "on-chip." They are merely "*connected via conventional inputs and output.*"

"These and other aspects of the invention may be obtained generally in a high accuracy, low power clock circuit for an integrated circuit which includes a high accuracy, crystal oscillator which *interfaces to an "off-chip" crystal to provide the high accuracy clock*, while an internal, low power oscillator provides a low power clock source. Either clock may be selected to drive the processor under program control. When high accuracy and stability are required, the crystal oscillator may be chosen as the processor clock, and when lower power is desired, the low power oscillator may be chosen as the processor clock while the high accuracy clock is disabled." (see Grundvig, col. 2, lines 29-40, *emphasis added*).

There is no teaching within Grundvig that the high accuracy oscillator 12 performs any "determining a frequency of the output signal of from the external oscillator (12) when the operational mode of the semiconductor device substantially comprises a low power oscillator bypass mode" as the Examiner seems to assert.

Here, the Applicant respectfully believes that the Examiner is asserting that it is the "high accuracy oscillator 12" determines the frequency of the output signal from the ""“off-chip" crystal (or external clock) 10," as taught within Grundvig.

In contradistinction, Grundvig merely teaches a first mode (high accuracy and stability) and a second mode (lower power). When operating in the first mode (high accuracy and stability) (which the Applicant believes the Examiner is comparing to the "low power oscillator bypass mode" of the Applicant's claimed subject matter), Grundvig does not teach the limitations of the Applicant's claimed subject matter within the claim 46 that include:

"determining a frequency of the output signal from the external oscillator when the operational mode of the semiconductor device substantially comprises a low power oscillator bypass mode;

determining whether the frequency of the output signal from the external oscillator substantially comprises a frequency that is suitable for use as a main system clock by at least one circuitry portion within the semiconductor device; and

processing the output signal, from the external oscillator, to generate a new clock signal that substantially comprises a frequency that is suitable for use as the main system clock."

When Grundvig operates in the first mode (high accuracy and stability), the signal provided from the ""off-chip" crystal (or external clock) 10" that is merely *interfaced* to the "high accuracy oscillator 12," and that signal is *simply used* by the device (i.e., by the IC 100)! There is no "determining whether the frequency of the output signal from the external oscillator substantially comprises a frequency that is suitable for use as a main system clock by at least one circuitry portion within the semiconductor device."

As also cited above, Grundvig discloses that "[t]he *interface* to the "off-chip" crystal (external clock) 10 provides the necessary high accuracy *frequency stability* for the high accuracy oscillator 12 *to act as a clock* for the IC 100." This interface is employed for *frequency stability*, in that, the ""off-chip" crystal (external clock) 10" provides a very reliable, accurate clock signal that is merely brought onto the "chip;" the "high accuracy oscillator 12" then merely relays this received clock signal so that it may "act as a clock for the IC 100." There is no teaching in Grundvig that the "high accuracy oscillator 12" operates to perform any "processing" of the signal received from the ""off-chip" crystal (external clock) 10" to generate a new clock that is suitable for use as a main system clock.

In Grundvig, there is also simply no "determining" by the "high accuracy oscillator 12" of whether the output signal from the ""off-chip" crystal (external clock) 10" comprises a frequency that is suitable for use as a main system clock by at least one circuitry portion within the "IC 100." As clearly stated within Grundvig, there is merely an "interface" between the ""off-chip" crystal (external clock) 10" and the "high accuracy oscillator 12" that is implemented using "*conventional inputs and outputs*."

Within Grundvig, when operating in the first mode (high accuracy and stability), the signal provided from the "high accuracy oscillator 12 *in combination with* the "off-chip" crystal (or external clock) 10" is merely employed within the IC 100; there is no

step of determining of whether it is suitable for use; it is merely used in this particular operational mode as disclosed within Grundvig!

As such, the Applicant respectfully asserts that the combination of Kohlschmidt and Grundvig fails to teach and disclose each and every element of the subject matter as claimed by the Applicant in claim 46 of a frequency adaptable method, comprising: starting up a semiconductor device; starting up an external oscillator, the external oscillator being communicatively coupled to the semiconductor device; providing an output signal from the external oscillator to the semiconductor device; determining an operational mode of the semiconductor device; determining a frequency of the output signal from the external oscillator when the operational mode of the semiconductor device substantially comprises a low power oscillator bypass mode; determining whether the frequency of the output signal from the external oscillator substantially comprises a frequency that is suitable for use as a main system clock by at least one circuitry portion within the semiconductor device; and processing the output signal, from the external oscillator, to generate a new clock signal that substantially comprises a frequency that is suitable for use as the main system clock.

The Applicant respectfully asserts that the inclusion of the Grundvig reference does not overcome the deficiencies of the Kohlschmidt with respect to claims 46-49.

The Applicant also respectfully believes that claims 47-49, being further limitations on the subject matter as claimed by the Applicant in claim 46, are also allowable.

As such, the Applicant respectfully requests that the Examiner withdraw the rejections to claims 46-49 under 35 U.S.C. § 103 (a) as being unpatentable over Kohlschmidt in view of Grundvig.

Allowable Subject Matter

9. In the above-referenced OA, the Examiner objected to claims 2-4, 6-8, 10, 34, 37-40, and 50 as being dependent upon a rejected base claim, but the Examiner indicated that these claims would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

The Applicant also respectfully requests that the Examiner withdraw the objections to claims 2-4, 6-8, 10, 34, 37-40, and 50 as being dependent upon a rejected

base claim in lieu of an allowance of the corresponding base claims from which they depend either directly or interveningly.

10. In the above-referenced OA, the Examiner stated that claims 11-20, 21-30, 41-45, and 51-55 are allowed.

The Applicant respectfully believes that claims 1-55 are in condition for allowance and respectfully requests that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present patent application.

RESPECTFULLY SUBMITTED,

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